

31046 U.S. PTO

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05/09/02

U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10063737	05/09/2002	716	1	2825	Bowers

**APPLICANTS: Hsu Jimmy;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

TAIWAN 91102057 02/06/2002 bb

PG-PUB DO NOT PUBLISH ☐RESCIND ☐

Foreign priority claimed

☒ yes ☐ no

35 USC 119 conditions met

☒ yes ☐ no

Verified and Acknowledged Examiners's initials bb

ATTORNEY DOCKET NO

8727-US-PA

TITLE : Voltage reference circuit layout inside multi-layered substrate

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
		Sheets Drwg.	Figs. Drwg.
		Print Fig.	
ISSUE FEE		Application Examiner	
Amount Due	Date Paid		
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	
		WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	

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